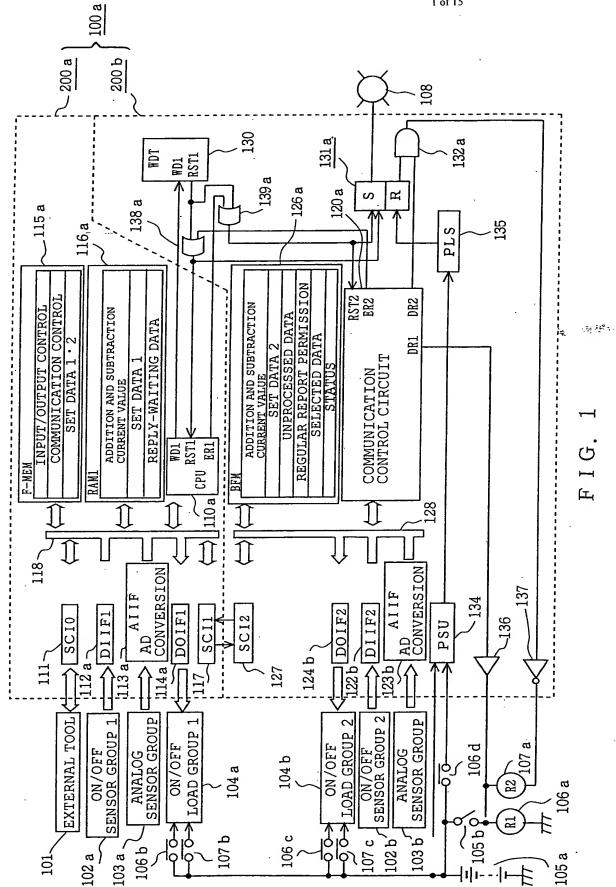
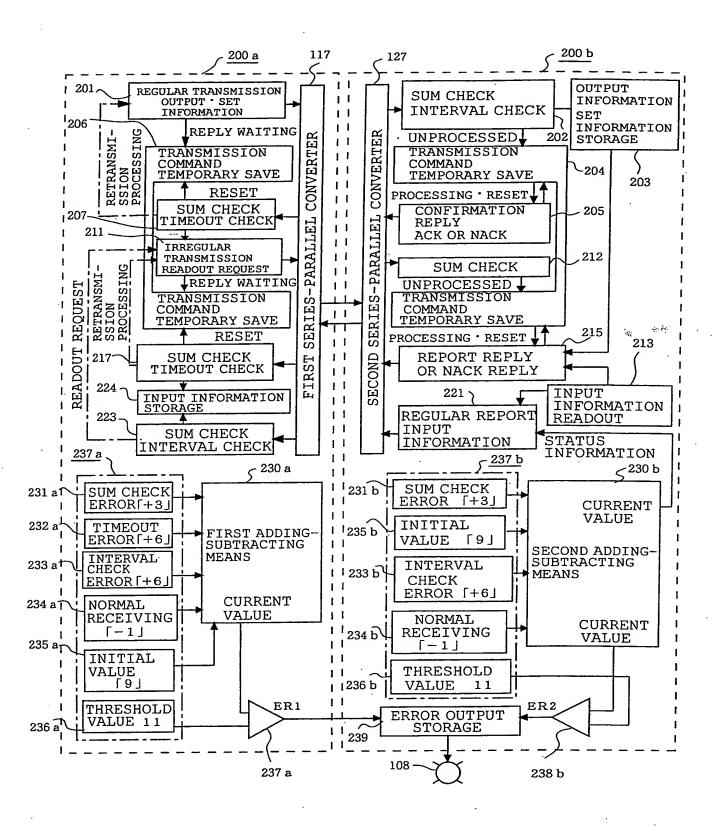
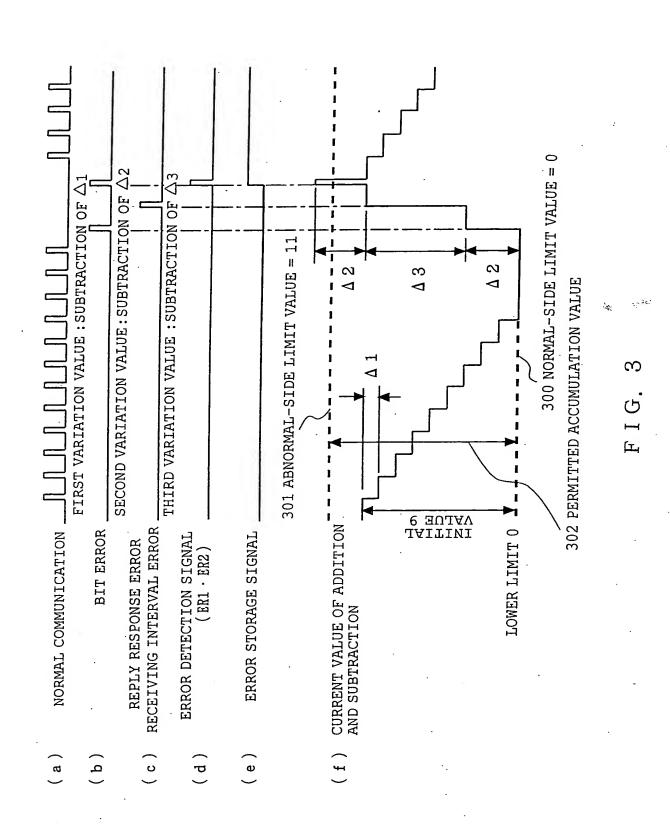
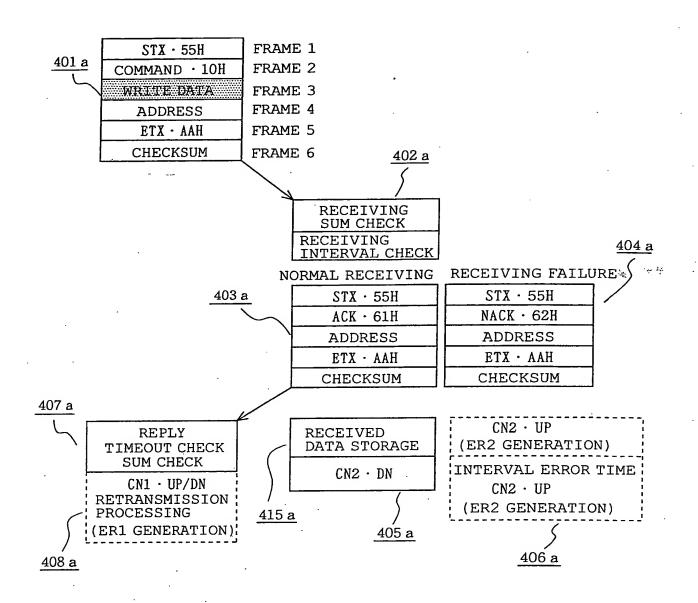
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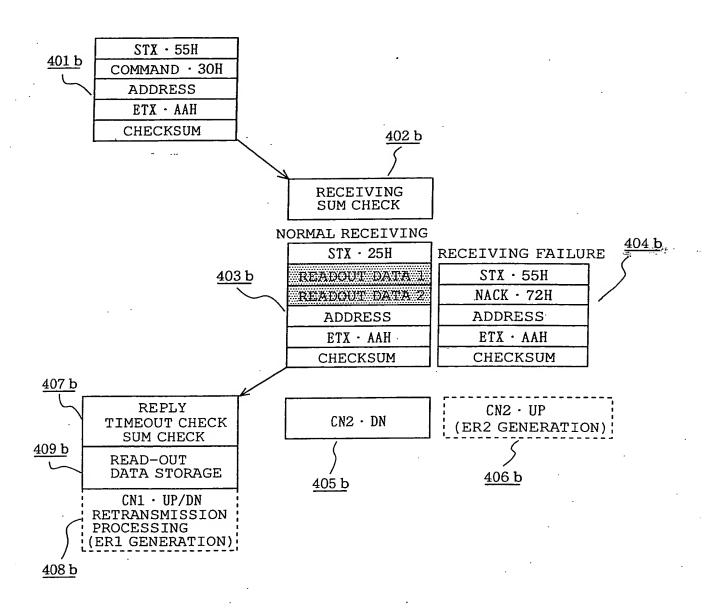




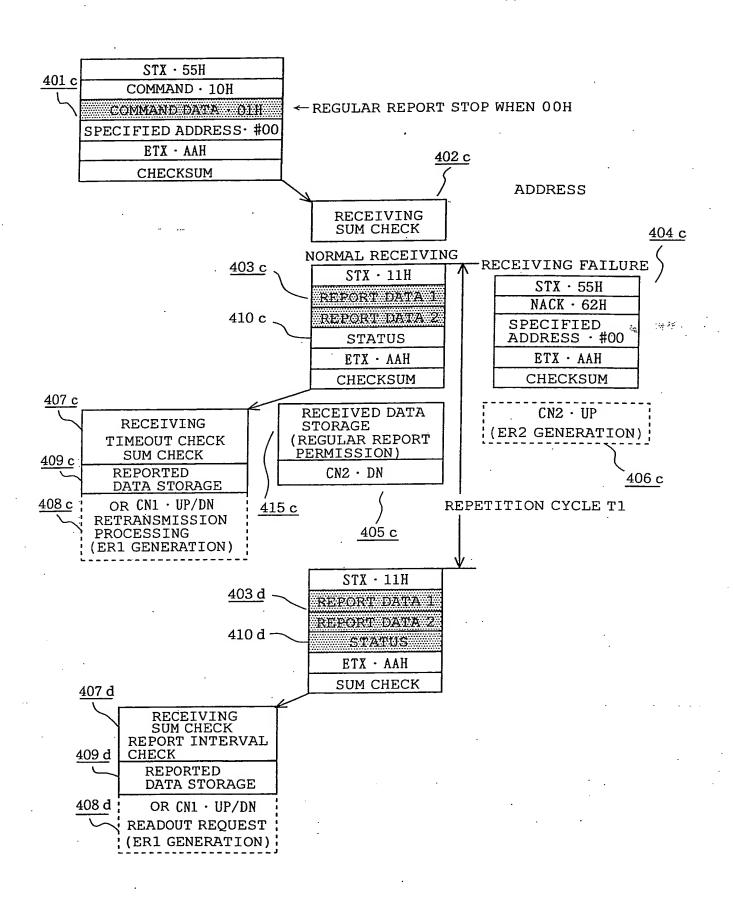
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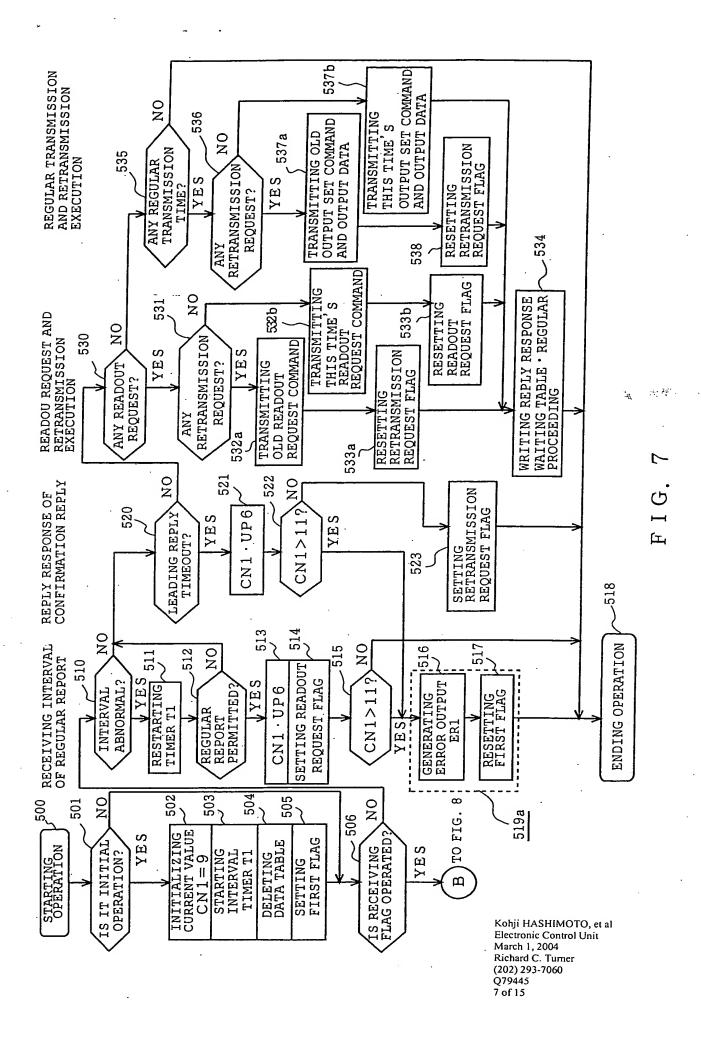


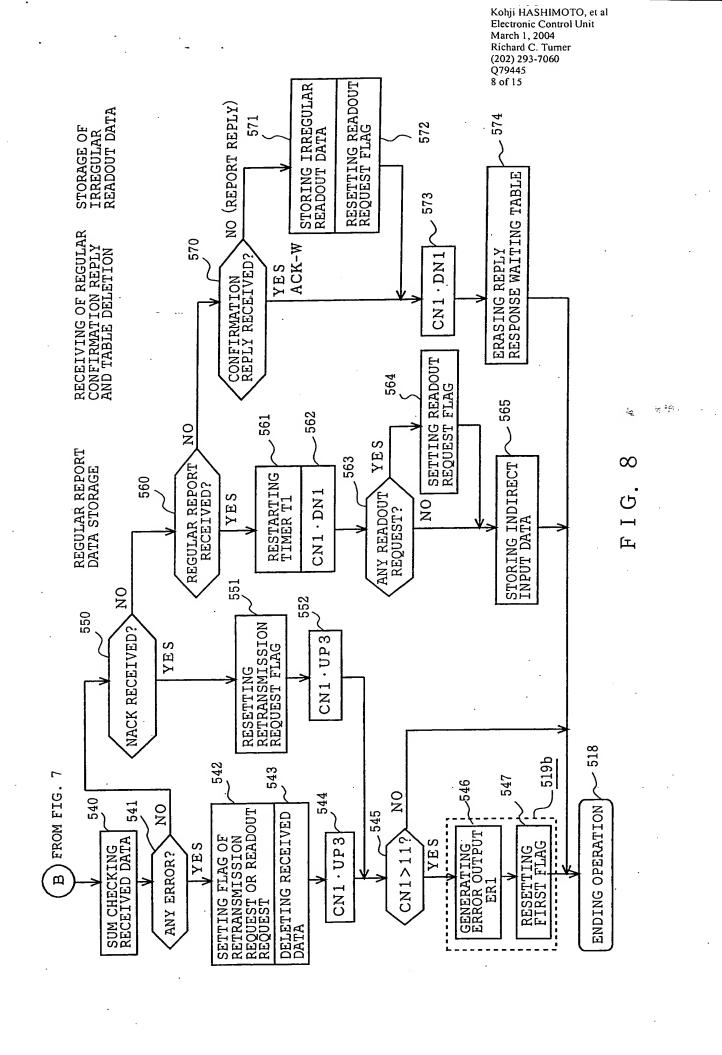
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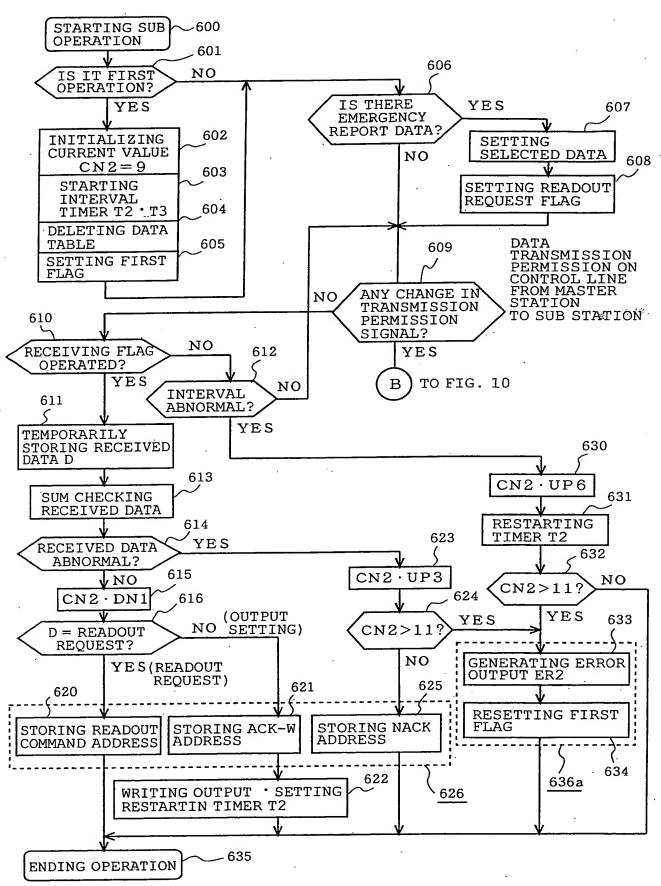
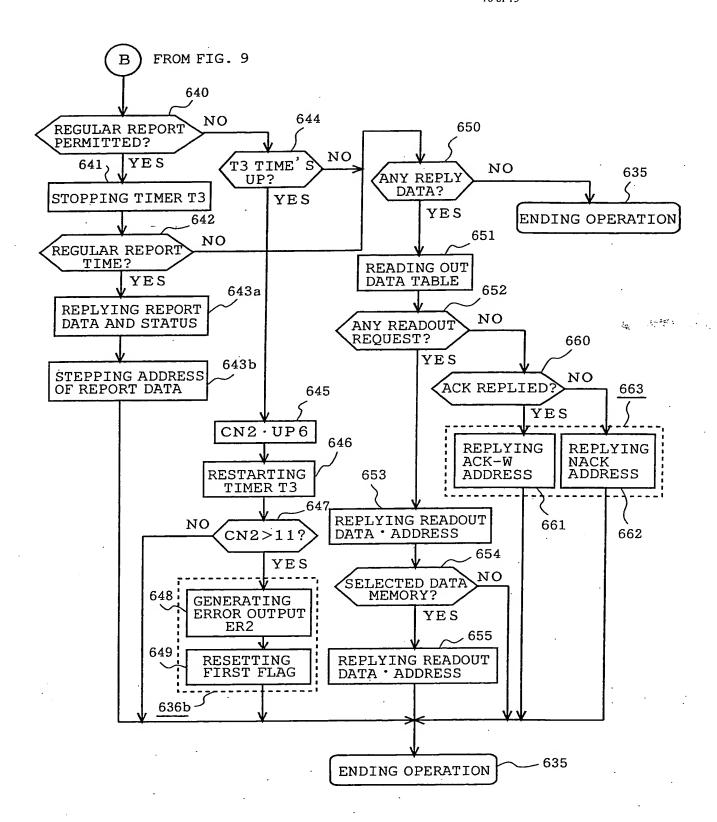
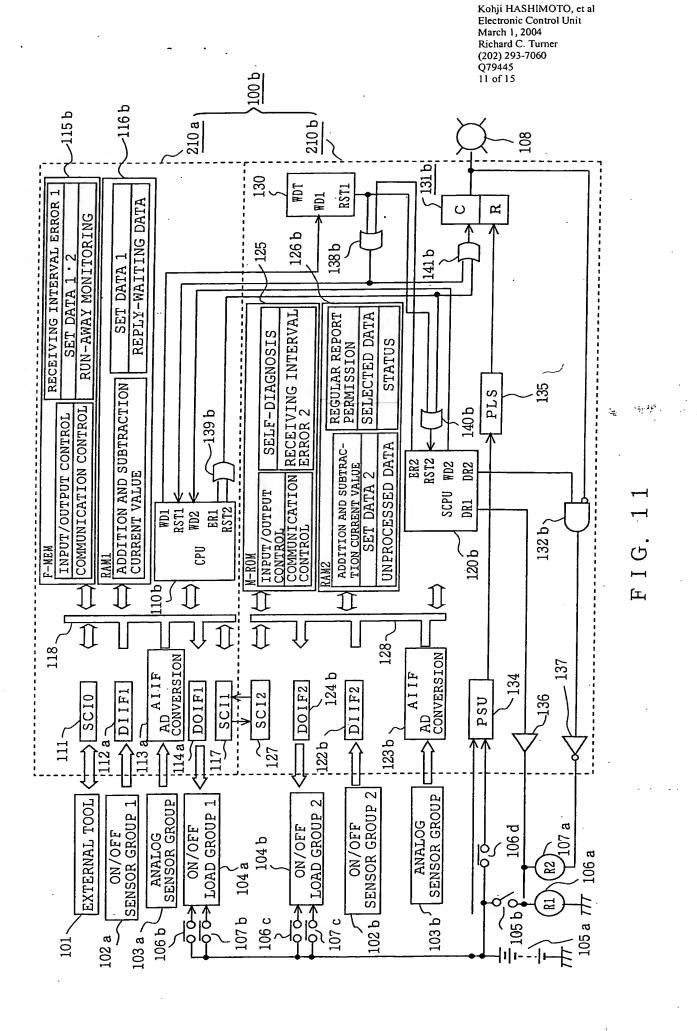


FIG 9

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	REGULAR REPORT PERMISSION	NORMAL-SIDE LIMIT VALUE	ABNORMAL-SIDE LIMIT VALUE	INITIALIZATION VALUE	FIRST VARIATION VALUE	SECOND VARIATION VALUE	THIRD VARIATION VALUE	REPLY RESPONSE ACCEPTABLE TIME PERIOD	RECEIVING INTERVAL ACCEPTABLE TIME PERIOD		INDIRECT OUTPUT 1	INDIRECT OUTPUT 2	
Р0	·				-		-				DR1	Y10	SMISSION ORDER IS ALTERNATE OF 0A AND 0B
b2 b1											DR2	Y12 Y11 Y10	ALTE
											Y02		IR IS
b4 b3											Y03	Y13	N ORDI ND 0B
p4											Y04	Y14	SMISSION ORDI OF OA AND OB
p 2	•										Y05	Y15	ANSMI ON OF
9 ['] q						,					Y06	Y16	AR TR MISSI
P2											Y07	Y17	REGULAR TRANS TRANSMISSION
ADDRESS	00	01	00	03	04	02	90		80	60	0A	08	щ.,

 $olimits_{\mathcal{O}}$

	STATUS MEMORY		INDIRECT OUTPUT 1	INDIRECT OUTPUT 2	ANALOG 1		ANALOG 2		ANALOG 3		ANALOG 4	٠	ANALOG 5	·	SELECTED DATA MEMORY		
p 0	G E		X00	<u>Х</u> 10													
p1	NA NO TION		X01	X11												ERROR CODE	
p2	ADDITION AN SUBIRACIION CURPENT VALI	HO	X02	X12	UPPER 8 BITS	LOWER 8 BITS	UPPER 8 BITS	S	ß	S	UPPER 8 BITS	LOWER 8 BITS	UPPER 8 BITS	LOWER 8 BITS		ERRO	
b4 b3	AT SU CU		X03	X13				LOWER 8 BITS	UPPER 8 BITS	LOWER 8 BITS					ADDRESS		
р4	RESS		X04	X14	PPER	OWER	ADDI	N									
p2	FLAG INPUT ADDRESS	HO.	X05	X15	D .	П	U .	I	n	I	n .	I		I		BIT SECTION	
p2 p6	OGNI		X06	Х16												BITS	
	FLAG		X07	X17													
DDRESS	10		11		12		13		14		15		16		17		

FIG. 13

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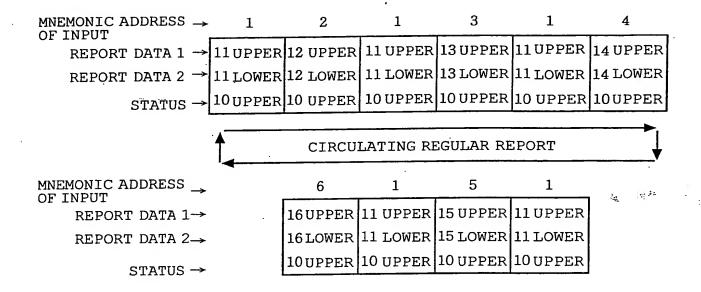


FIG. 14

